**ATD Control Register 5 (ATDCTL5)**

This register selects the type of conversion sequence and the analog input channels sampled. Writes to this register will abort current conversion sequence and start a new conversion sequence. If external trigger is enabled (ETRIGE = 1) an initial write to ATDCTL5 is required to allow starting of a conversion sequence which will then occur on each trigger event. Start of conversion means the beginning of the sampling phase.

1 Maximum ATD conversion clock frequency is 2 MHz. The maximum allowed bus clock frequency is

shown in this column.

**Min. Bus Clock2**

2 Minimum ATD conversion clock frequency is 500 kHz. The minimum allowed bus clock frequency is

shown in this column.